Tunnel Field-Effect Transistors Based on InP-GaAs Heterostructure Nanowires

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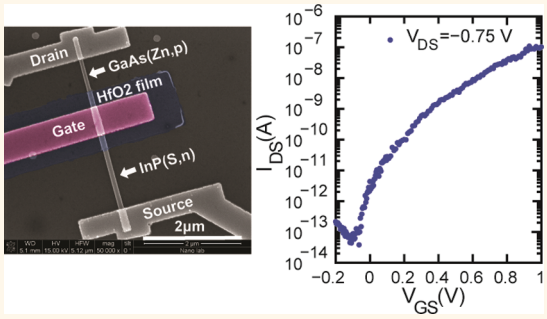
ABSTRACT



We present tunneling field-effect transistors fabricated from InP-GaAs heterostructure nanowires with an *n-i-p* doping profile, where the intrinsic InP region is modulated by a top gate. The devices show an inverse subthreshold slope down to 50 mV/dec averaged over two decades with an on/off current ratio of approximately 10^7 for a gate voltage swing (V_{GS}) of 1 V and an on-current of 2.2 μA/μm. Low-temperature measurements suggest a mechanism of trap-assisted tunneling, possibly explained by a narrow band gap segment of InGaAsP.

KEYWORDS: nanowire · tunnel transistor · heterostructure · InP · GaAs · MOSFET

The tunnel field-effect transistor (TFET) belongs to the family of so-called steep-slope devices that are currently being investigated for ultra-low-power electronic applications.[1−3] The concept has been explored in several material systems based on semiconductor *p-i-n* junctions,[4−7] carbon nanotubes,[8] and semiconductor nanowires.[9−12] A key feature of the TFET, which is critical for low-power switching, is the possibility for an inverse subthreshold slope, *S*, below the limit of 60 mV/dec for normal FETs.[4,8] The fundamental challenge for realizing commercially competitive TFETs is a limited on-current level, which is typically addressed by creating higher doping levels and abrupt doping profiles. However, this may negatively affect the off-state properties due to a pronounced Urbach tail in the density of states, with a high density of impurity levels in the band gap.[13]

Some heterostructures offer a staggered band alignment, allowing a steeper band structure profile over the junction than that achievable by using doping modulation only. Such structures are currently being investigated as a means to boost TFET performance.[14,15] Additionally, using a smaller band gap material in the source is predicted to significantly enhance the tunnel current.[16] In this respect, the III−V semiconductors are highly interesting, as they typically have low effective carrier masses and, in contrast to Si and Ge, direct band gaps that allow for efficient tunneling.[17] A few special heterostructures, such as InAs and GaSb, even have broken band lineups, whereby the band-to-band transport occurs without any barrier.[12,18,19]

Semiconductor nanowires are particularly attractive for TFET research, as they allow for heteroepitaxy of lattice mismatched materials, and the geometry of the structure also facilitates wrap-gate formation to the active region of the device.[20]

For nanowires scaled to the 1D transport regime, the TFET device properties are also believed to be improved,[14] however, under the assumption that the surface properties can be controlled. Recent developments in nanowire growth and doping control have allowed studies of band-to-band tunneling in Si nanowires,[9,10] in InP-GaAs heterostructure nanowires,[21] and in bulk Si to InAs nanowire interfaces.[15] However, considerable work is still required to realize competitive nanowire-based TFETs, and many questions regarding the actual tunnel mechanism in such devices are not fully answered.

In this work we have studied the reverse bias properties of heterostructure InP (n^+-*i*)-GaAs (p^+) nanowires. The nanowires (NWs) were processed into TFETs by aligning omega-shaped top gates to the intrinsic InP segments, and source and drain contacts to the *n*/*p* segments. In reverse bias, the

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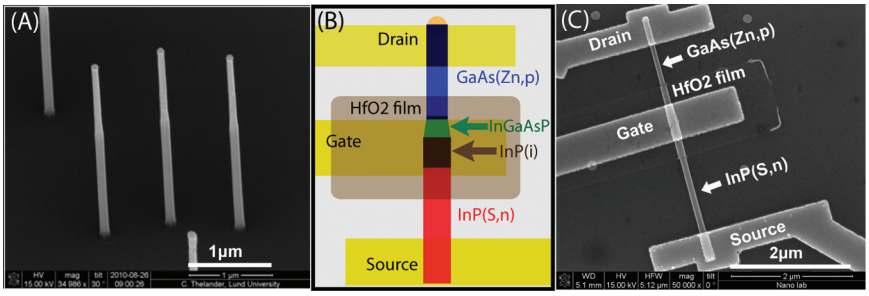

Figure 1. (A) SEM image of as-grown nanowires (30° tilt). (B) Schematic diagram of the InP-GaAs NW-TFET. (C) SEM top view of a fabricated device.

transistors show a band-to-band tunneling current up to 100 nA at $V_{DS} = -0.75$ V (1.1 μA/μm) with an on/off current ratio (I_{ON}/I_{OFF}) of approximately 10^7 for a V_{GS} swing of 1 V. We find that both on-current and subthreshold slope are improved compared to previously reported nanowire TFETs based on epitaxially grown nanowires.[9,10] A minimum inverse subthreshold slope of around 50 mV/dec was observed close to pinch-off, averaged over a gate voltage range of 100 mV (two decades). The temperature dependence of the transfer characteristics indicates that the tunneling current consists of a trap-assisted tunneling (TAT) component and a band-to-band tunneling (BTBT) component.

RESULTS AND DISCUSSION

A SEM micrograph of as-grown nanowires is shown in Figure 1A. The epitaxial growth resulted in nanowires about 4 μm long, with roughly 2.5 μm long InP sections (100 nm diameter) and 1.5 μm long GaAs sections (85 nm diameter). The nominally intrinsic InP segment had a length of 200−300 nm. As a result of metallurgical interactions of the growth species with the Au seed particle when switching both group III and V elements simultaneously, a segment of narrow band gap InGaAsP is formed in the heterostructure region. This was observed by Wallentin *et al.* in the growth of corresponding tunnel diode structures and was suggested to contribute to the high band-to-band tunnel current density obtained for such diodes.[21] The InGaAsP region is seen as the tapered region in Figure 1A.

SEM image of a fabricated device with an aligned top gate that covers the intrinsic InP region, and the transition region is shown in Figure 1C.

A schematic band diagram of an InP-GaAs heterostructure is shown in Figure 2A, based on the material composition and estimated doping levels discussed in ref 21 (*n*-InP: 3×10^{18} cm^{-3}, *i*-InP: 1×10^{15} cm^{-3}, *p*-GaAs: 1×10^{19} cm^{-3}). The band diagram was created using a Poisson solver[22] with band offsets as reported by Pistol and Pryor.[23]

Electrical measurements were performed on individual devices under vacuum and dark conditions at room temperature. In all n^+-*i*-p^+ devices the *n*-side was grounded and the drain voltage, V_{DS}, was applied to the *p*-side. The diode $I_{DS}-V_{DS}$ curve of a heterostructure nanowire with no fabricated gate is shown in Figure 2B. As no gate is present, the applied voltage at reverse bias drops over both the heterostructure and the intrinsic region of the nominally undoped InP segment, thus not giving conditions for BTBT. The corresponding $I_{DS}-V_{DS}$ output characteristics of a 3-terminal (top-gated) device are shown in Figure 3A. As a result of the device design, the top gate was observed to affect both the reverse and the forward current levels. For a reverse (negative) V_{DS}, a positive gate voltage (V_{GS}) is used to shift the conduction band of the InP-*i* segment in such a way that band-to-band tunneling is possible. In the case of a positive (forward) V_{DS}, an applied gate voltage leads to electron accumulation or depletion on the InP side of the junction. For negative V_{GS} the InP (*i*)-segment becomes depleted, which extends the depletion region and prevents band-to-band tunneling. Instead the device behaves like a rectifying *p-n* junction, where the negative gate bias increases the reverse breakdown current and lowers the ideality factor in the forward direction. The onset voltage approaches that of an ideal diode, *i.e.*, the band gap minus the InP-GaAs band offset. For positive V_{GS} we observed a similar onset of forward current ($V_{DS} = 0.25$ V), as in the case of the heavily doped n^+-p^+ diode studied,[21] although in this case without the region of negative differential resistance.

Figure 3B depicts the measured transfer characteristics of a fabricated device under reverse bias ($V_{DS} = -0.75$ V). We explain the strong dependence of I_{DS} on V_{GS} by band-to-band tunneling, where the tunneling probability increases for increasing positive V_{GS}. An on/off current ratio close to 10^7 was observed at $V_{DS} = -0.75$ V for a V_{GS} swing of 1 V. For the same device at $V_{DS} = -0.85$ V and $V_{GS} = 1$ V, an on-current of 2.2 μA/μm was obtained. At $V_{DS} = -0.75$ V, a minimum inverse subthreshold slope, $S = -[\mathrm{d}(\log 10\ I_{DS})/\mathrm{d}V_{GS}]^{-1}$, of 50 mV/dec was observed close to pinch-off, where the slope was averaged over a range of 100 mV in gate voltage (Figure 3B). This value is below the $k_BT \ln 10/q \approx 60$ mV/dec subthreshold slope limit of conventional Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) (k_B, T, and q are the Boltzmann constant,

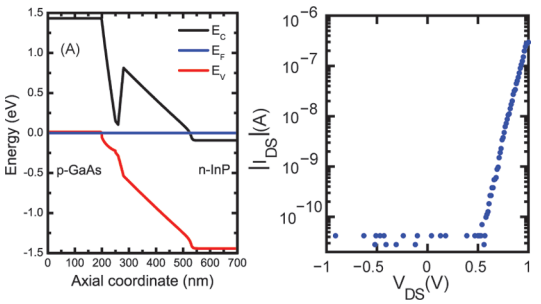

Figure 2. (A) Modeled energy band diagram of the nanowire with p^+-i-n^+ doping profile. (B) $I_{DS}-V_{DS}$ of a two-terminal device before top-gate fabrication, based on a p-i-n heterostructure nanowire.

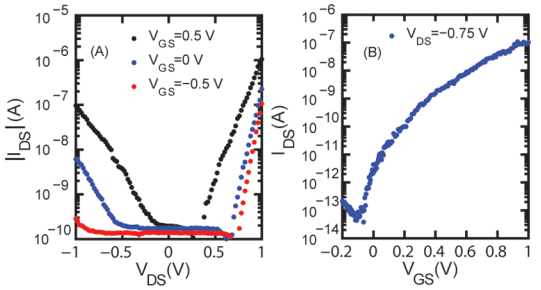

Figure 3. (A) Absolute value of I_{DS} *vs* V_{DS} of a fabricated device at three different V_{GS} of −0.5, 0, and 0.5 V. (B) Transfer characteristics of a device for a reverse bias of V_{DS} = −0.75 V.

the temperature, and the charge, respectively).[24] However, our measurements showed a distribution in inverse subthreshold slope between devices from 50 to 80 mV/dec. The average slope for V_{GS} = 0 to 1 V was 150 mV/dec, which is an improvement compared to other reported nanowire tunnel FET concepts based on epitaxially grown NWs.[9,10] The low S demonstrates an excellent gate control, which indicates a surprisingly high-quality interface between InP and HfO_2 for the process conditions used. Recently, our group has demonstrated regular NW-FETs with S close to the thermal limits, which were also based on omega-gated InP NWs.[25]

The temperature dependence of the subthreshold slope is a useful probe to investigate possible transport mechanisms contributing to the observed reverse-biased transfer characteristics.[7,8,10] For this reason, $I_{DS}-V_{GS}$ measurements were performed at different temperatures for V_{DS} = −0.7 V for the device shown in the inset of Figure 4. Figure 4A depicts the transfer characteristics of a fabricated device at different temperatures between 100 and 300 K in steps of 20 K. Three regions with different V_{GS} dependence can be identified corresponding to onset of various transport mechanisms. At the OFF state (negative V_{GS}) the main transport mechanism is Schockley−Read−Hall recombination in a reverse biased p^+-i-n^+ diode, which should be strongly temperature dependent. However, as the OFF current (I_{OFF}) was close to the instrument sensitivity limits already at room temperature, such a temperature dependence could not be confirmed.

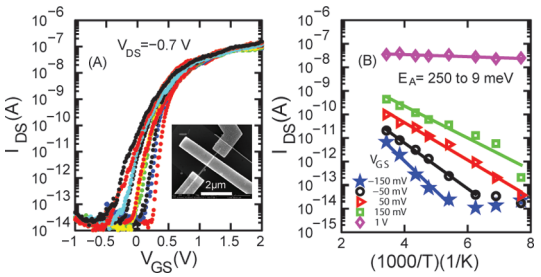

Figure 4. (A) Transfer characteristics for reverse bias V_{DS} = −0.7 V at temperatures ranging from 100 to 300 K in steps of 20 K. For V_{GS} < 0.4 V the subthreshold current is strongly temperature dependent. However, at higher gate voltage the drain current is temperature independent, confirming the presence of direct BTBT. Inset: SEM image of the corresponding device (NWs grown with 40 nm Au particle). (B) Arrhenius plots of TFET extracted at V_{DS} = −0.70 V for different gate voltages. The extracted activation energies indicate that transport mechanisms are driven by TAT and direct BTBT at the low and high gate bias, respectively.

For 100 K < T < 300 K and intermediate gate bias (V_{GS} < 0.4 V) a strong temperature dependence of the drain current was observed. The strong temperature dependence cannot be explained only with a change in band gap and band offset with temperature. Similar device behavior has been reported by others,[7,10] in which case trap-assisted tunneling was proposed as a possible transport mechanism, where electrons first tunnel into a trap within the band gap, from which they are thermally excited into the conduction band. In our case, the narrow band gap section of InGaAsP as observed by X-ray energy dispersive spectroscopy may act as a trap for the electrons at low temperatures, thereby improving the subthreshold properties. Such a trap-assisted tunneling mechanism is supported by the results of Arrhenius plots made for different gate voltages (Figure 4B) where an activation energy of 0.25 eV is extracted for the subthreshold region (V_{GS} = −0.15 V). A possible future study, aimed at verifying this interpretation, could be based on InAs-GaAs heterostructure nanowires, for which the narrow band gap section is completely eliminated.

The temperature dependence observed in this region may also be explained by band tailing associated with high doping levels,[26] known from studies of optical properties of III−V semiconductors, such as GaAs.[27,28] Such states may extend to energies within the band gap, resulting in an exponential extension of the density of states in the below band-edge region. The slope of the so-called Urbach tail, which is the exponential part of the absorption edge, may therefore be one explanation for the temperature dependence of the subthreshold region observed here. However, further studies are necessary to confirm this interpretation.

For V_{GS} > 0.5 V (ON state), only a very weak temperature dependence of the drain current is observed. An activation energy of 9 meV is extracted at V_{GS} = 1 V, confirming the presence of direct band-to-band tunneling in the device at higher gate voltages.

A few devices with a variation in gate−heterojunction overlap were fabricated. Here we found that in cases where the gate did not cover the entire tapered region (gate−drain underlap) the inverse subthreshold slope was degraded. As expected, gate control of the InGaAsP transition region appears critical to the device performance (see Supporting Information).

CONCLUSIONS

We have demonstrated single nanowire InP-GaAs tunneling FETs with minimum S of 50 mV/dec and I_{ON}/I_{OFF} of 10^7. A strong temperature dependence of the subthreshold current indicates trap-assisted tunneling and thermal emission from traps. For positive gate voltages the temperature dependence is found to be considerably weaker, indicating direct band-to-band tunneling. These results demonstrate the versatility of III−V NW heterostructures as building blocks in future low-power electronics. It is expected that the TFET performance could be further enhanced with reduced diameters, with optimized doping profile, and by designing gates that fully wrap around the intrinsic device region.

METHODS

Samples were prepared for nanowire growth by depositing 40 and 80 nm Au particles in a density of 0.2 μm^{-2} on InP (111)B substrates by an aerosol technique.[29] The nanowires were grown in a low-pressure (100 mbar) metal organic vapor phase epitaxy system with a total flow of 6 L/min using hydrogen (H_2) as carrier gas. For InP growth, trimethylindium (TMI) and phosphine (PH_3) were used as precursors, with constant molar fractions of $\chi_{TMI} = 3.5 \times 10^{-6}$ and $\chi_{PH3} = 6.25 \times 10^{-3}$. Hydrogen sulfide ($H_2S$) was added as n-type doping precursor[30] at a molar fraction of $\chi_{H2S} = 7.1 \times 10^{-6}$. For the GaAs section, trimethylgallium (TMG) and arsine (AsH_3) were used at molar fractions of $\chi_{TMG} = 5.2 \times 10^{-6}$ and $\chi_{AsH3} = 0.55 \times 10^{-3}$. DEZn was here used as a GaAs NW p-dopant precursor[31] in a molar fraction of $\chi_{DEZn} = 2.9 \times 10^{-7}$. Finally, hydrogen chloride (HCl) at a molar fraction of $\chi_{HCl} = 15.0 \times 10^{-6}$ was used to control the radial growth.[32] The samples were first annealed at 550 °C for 10 min under a PH_3/H_2 gas mixture to desorb any surface oxides. The reactor was then cooled to a temperature of 420 °C, at which point growth was initiated by adding TMI. After a 15 s nucleation time, HCl and H_2S were added, after which n-type InP growth was continued for 9 min. Then H_2S was switched off and one minute of nominally intrinsic InP was grown. GaAs growth was initiated by simultaneously switching group III, group V, and dopant precursors. After 10 min, growth was interrupted and the sample was cooled in a PH_3/H_2 gas mixture.

After growth, nanowires were broken off and transferred to doped Si samples capped with a 100 nm thick SiO_2 thermal oxide. The locations of selected nanowires were then determined relative to predefined metal markers using a scanning electron microscope. The samples were spin-coated in PolyMethylMethAcrylate (PMMA), followed by electron beam lithography exposure of a window that was aligned to the InP(i) segment and partially overlapping InP(n^+) and GaAs(p^+) segments. A high-κ HfO_2 film was formed by atomic layer deposition of Tetrakis[DiMethylAmino]Hafnium (TDMAHf) and H_2O at 100 °C, followed by lift-off. Gate and contact to n^+-type InP were fabricated in a single EBL step, where the InP segments were etched with H_3PO_4/H_2O (1:9) for 2 min and then with H_2SO_4/H_2O (1:3) for 1 min, followed by sulfur passivation for 10 min. A Ti/Au (20/80 nm) metal combination was used as the contact materials.

After another EBL step, the GaAs p^+-segments were etched in an HCl/H_2O (1:1) solution for 10 s, followed by a 2 min surface passivation in an $(NH_4)_2S_X$ solution. A Pd/Zn/Pd (10/10/80 nm) metal combination, which is known to give ohmic contacts to p-GaAs NWs,[21] was used. Figure 1B and C show a schematic diagram and an SEM image of a fabricated device with an aligned top gate that covers the intrinsic InP region and the transition region (the tapered section).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: $I_{DS}-V_{DS}$ characteristics of two-terminal devices of InP and GaAs segments that show low-ohmic behavior, transfer characteristics of a device with gate−drain underlap, and gate leakage current. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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